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A Low-Power High-Speed Sense-Amplifier-Based Flip-Flop in 55nm MTCMOS

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ABSTRACT-A sense-amplifier-based flip-flop (SAFF) suitable for low-power high-speed operation. With the employment of a new sense-amplifier stage as well as a new single-ended latch stage, the power and delay of the flip-flop is greatly reduced. The proposed SAFF can provide low voltage operation by adopting MTCMOS optimization. The proposed SAFF delay and the power are smaller than those of the existing master-slave flip-flop (MSFF). The power-delay-product of the proposed SAFF improves compared with the conventional SAFF and MSFF, respectively the area of the proposed flip-flop decrease, the proposed SAFF could provide robust operation even low power supply voltages. But in this design we are using 45nm technology by using this technology we can get the required output by giving 1LVT (low threshold voltage).

KEYWORDS: Light fidelity, wireless fidelity, data transmission.

I. INTRODUCTION

High speed and low power is the theme of digital circuits. As basic storage elements, the delay and power of the flipflops directly determines the performance and power of digital systems. As described in [1], flip-flops contribute a significant portion of the power consumption of the digital system. Moreover, the setup-time and CK-to-Q delay of the flip-flop directly affects the maximum clock frequency of the system. Therefore, optimizing the delay and power of flip-flops can directly improve the performance and reduce the power consumption of digital systems. The most commonly used flip-flop in digital systems is the master–slave flip-flop (MSFF). The schematic of the C2MOS [2] master-slave flip-flop in the SMIC 55 nm standard cell library provided by the foundry is shown in Figure 1. As shown in Figure 1, the data should pass through the first latch before the rising edge of CK, which ensures that the flip-flop can capture the correct data at the rising edge of CK. Therefore, the setup time in the MSFF is relatively long. At the same time, the CK-to-Q delay involves several logics and is also relatively large.Since the embedded system is dedicated to specific tasks, design engineers can optimize it, reducing the size and cost of the product, or increasing the reliability and performance. Some embedded systems are mass-produced, benefiting from economies of scale.

Physically embedded systems range from portable devices such as digital watches and MP3 players, to large stationary installations like traffic lights, factory controllers, or the systems controlling nuclear power plants. Complexity varies from low, with a single microcontroller chip, to very high with multiple units, peripherals and networks mounted inside a large chassis or enclose

II.LITERATURE SURVEY

[1]Jeong, H.; Oh, T.W.; Song, S.C.; Jung, S.-O. Sense-amplifier-based flip-flop with transition completion detection for low-voltage operation. 2018.

A high-speed and highly reliable sense amplifier-based flip-flop with transition completion detection (SAFF-TCD) is low supply voltage (VDD) operation. The SAFF-TCD adopts the internally generated detection signal to indicate the completion of sense-amplifier stage transition. The detection signal gates the pull-down path of the sense-amplifier stage and the slave latch, thus overcoming the operational yield degradation, current contention, and glitches of previous SAFFs.

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Summary: From this article, I have considered the concept of the current contention, and glitches free of SAFFs. [2]Jeong, H.; Park, J.; Song, S.C.; Jung, S.-O. Self-Timed Pulsed Latch for Low-Voltage Operation With Reduced Hold Time. IEEE J. Solid-state Circuits 2019.

A self-timed pulsed latch (STPL) is proposed for low VDD operation. By comparing input and output, the transparency window is adaptively generated in STPL, which resolves the hold time problem of the conventional pulsed latch.

Summary: From this article, I have considered the concept of hold time and setup time and conventional pulsed latch problem

[3]Kim, J.-C.; Jang, Y.-C.; Park, H.-J. CMOS sense amplifier-based flip-flop with two N-C2MOS output latches. Electron. Lett. 2000, 36, 498–500.

Nikolic's flip-flop was proposed to further increase the operating speed. NAND SR latch of [1] was replaced by a combined circuit of a cross-coupled inverter latch and two inverting buffers. However, the power consumption of the flip-flop is much larger than that of the conventional SAFF. In the new SAFF proposed in this work, the NAND SR latch in was replaced by two NC2 MOS latches. The new SAFF gave the fastest operating speed from among the flip-flops compared in this work, while the power consumption increased moderately compared to that of the conventional SAFF

Summary: From this article, I have considered Increases the operating speed more than the flip-flop a dynamic style circuit

III. PROPOSED SYSTEM

The schematic of the proposed SAFF is shown in Figure 5. As shown in Figure 5, the SAFF is composed of a SA stage and a slave latch, similar to the previous SAFFs. As described in previous sections, the SA stage could capture the data right after the rising edge of CK and the slave latch is applied to maintain the output during the negative half cycle of CK.



IV. WORKING PRINCIPLE

The structure of the SA is changed; the NMOS controlled by CK (MN5 in) is split into two (MN5 and MN6) and moved to connect directly to the back-to-back inverter, as shown in Figure. Through the conversion, the nodes related to MN3 and MN4 no longer need to charge during pre-charge operation since the transistors MN5 and MN6 are off when CK is low. Since pre-charge power is an important part of the power consumption of the SAFF, the power consumption of the proposed SAFF can be greatly reduced.

V. RESULTS

The proposed SAFF has been designed based on **45** nm technology. In order to verify the validity of the proposed SAFF, the MSFF, the conventional SAFF, Nikolic's SAFF, Lin's SAFF and Jeong's SAFF have also been designed based on the same technology for comparison. With the same settings is adopted to perform all post-layout simulations for comparisons. The performance comparisons such as of the area, power consumption, CK-to-Q delay, setup time and hold time of the various flip-flops are described in detail below table.

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Power and delay comparison of Existing and Proposed SAFF

Type of SAFF	Power	Delay	Area
Nikolic's SAFF	5.54mw	9.84ms	28
Strollo's SAFF	7.12mw	9.60ms	24
Jeong's SAFF	130mw	9.90ns	26
Lin's SAFF	2.21mw	1.143ms	20
Proposed SAFF	2.40mw	1.02ns	22

Designs, waveforms and output screenshots:



FIGURE 2 : Schematic of the proposed SAFF is shown in the figure



Figure 3 :Wave forms for proposed SAFF

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VI. ACKNOWLEGMENT

I would like to thank my guide Asst. Prof. CH. Murali Krishna for supporting me in different phases of this project. Also I thank Siddharth institute of Engineering and Technology for providing me all resources.

VII.CONCLUSION

A low-power high-speed SAFF is proposed in this paper. A new structure for the SA stage is proposed to minimize the pre-charge power of the SAFF. Additionally, a glitch-free and contention-free single-ended latch is proposed. With the employment of the new SA stage and the single-ended latch, the delay and power of the SAFF are greatly optimized. The power-delay-product of the proposed SAFF shows a $2.7 \times$ improvement compared with that of the conventional SAFF at a 25% input data toggle rate. The improvement is $3.55 \times$ when compared with the MSFF, which indicates that the proposed SAFF is a good choice for replacing MSFFs in digital systems to provide low-power, high-speed operation.

REFERENCES

[1]. Teh, C.K.; Fujita, T.; Hara, H.; Hamda, M. A 77% energy-saving 22-transistor single-phase-clocking D-flip-flop with adaptive-coupling configuration in 40nm CMOS. In Proceedings of the IEEE Int. Solid-State Circuits Conf, San Francisco, CA, USA, 20–24 February 2011.

[2]. Suzuki, V.; Odagawa, K.; Abe, T. ClockedCMOScalculator circuitry. IEEE J. Solid-State Circuits 1974, 8, 462–469.

[3]. Partovi, H.; Burd, R.; Salim, U.; Weber, F.; Digregorio, L.; Draper, D. Flow-through latch and edge triggered flipflop hybrid elements. In Proceedings of the IEEE International Solid-State Circuits Conference, Digest of Technical Papers, ISSCC. San Francisco, CA, USA, 8–10 February 1996.

[4]. Na_ziger, S.D.; Colon-Bonet, G.; Fischer, T.; Riedlinger, R.; Sullivan, T.J.; Grutkowski, T. The implementation of the Itanium 2 microprocessor. IEEE J. Solid-State Circuits 2002, 37, 1448–1460.

[5]. Alioto, M.; Consoli, E.; Palumbo, G. General Strategies to design nanometer flip-flops in the energy-delay space. IEEE Trans. Circuits Syst. I, Reg. Papers 2010, 57, 1583–1596.

[6]. Pan, D.; Ma, L.; Cheng, H.; Min, H. A Highly E_cient Conditional Feed through Pulsed Flip-Flop for High-Speed Applications. IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 2020, 28, 243–251

[7]. Matsui, M.; Hara, H.; Uetani, Y.; Kim, L.; Nagamatsu, T.; Watanabe, Y.; Chiba, A.; Matsuda, K.; Sakurai, T. A 200 MHz 13 mm 2D DCT macrocell using sense-amplifying pipeline flip-flop scheme. IEEE J. Solid-State Circuits 1994, 29, 1482–1490.

[8]. Montanaro, J.; Witek, R.; Anne, K.; Black, A.; Cooper, E.; Dobberpuhl, D.; Donahue, P.; Eno, J.; Hoeppner, W.; Kruckemyer, D.; et al. A 160-MHz 32-b 0.5-W CMOS RISC microprocessor. IEEE J. Solid-State Circuits 1996, 31, 1703–1717.

[9]. Nikolic, B.; Oklobdzija, V.G.; Stojanovic, V.; Jia, W.; Chiu, J.K.-S.; Leung, M.M.-T. Improved sense-amplifierbased flip-flop: Design and measurements. IEEE J. Solid-State Circuits 2000, 35, 876–884.

[10]. Kim, J.-C.; Jang, Y.-C.; Park, H.-J. CMOS sense amplifier-based flip-flop with two N-C2MOS output latches. Electron. Lett. 2000, 36, 498–500.

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[11]. Lin, J.-F.; Hwang, Y.-T.; Wong, C.-S.; Shey, M.-H. Single-ended structure sense-amplifier based flip-flop for low-power systems. Electron. Lett. 2015, 51, 20–21.

[12]. Strollo, G.M.; De Caro, D.; Napoli, E.; Petra, N.Anovel high-speed sense-amplifier-based flip-flop. IEEE Trans.Very Large Scale Integr. (VLSI) Syst. 2005, 13, 1266–1274.

1[3]. Jeong, H.; Oh, T.W.; Song, S.C.; Jung, S.-O. Sense-amplifier-based flip-flop with transition completion detection for low-voltage operation. IEEE Trans. Very Large Scale Integr. (VLSI) Syst. 2018, 26, 609–620.

[14]. Jeong, H.; Park, J.; Song, S.C.; Jung, S.-O. Self-Timed Pulsed Latch for Low-Voltage Operation with Reduced Hold Time. IEEE J. Solid-state Circuits 2019, 54, 2304–2315





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